WHAT IS CLAIMED IS:

1. A method for forming a bipolar transistor on a wafer, the wafer having a buried layer and an epitaxial layer of a first conductivity type formed over the buried layer, the epitaxial layer having a smaller dopant concentration than the buried layer, the method comprising the steps of:

forming a trench in the epitaxial layer;

forming a layer of base material on the epitaxial layer and the trench;

forming a layer of base protection material on the layer of base material;

chemically-mechanically polishing the epitaxial layer, the layer of base material, and the layer of base protection material until a top surface of the epitaxial layer and a top surface of the layer of base protection material are substantially coplanar;

forming an isolation region on the layer of base material and the layer of base protection material; and

removing a portion of the layer of base protection material to expose a portion of the layer of base material.

2. The method of claim 1 wherein the portion of the layer of base protection material is removed with a wet etch.

3. The method of claim 2 wherein an area and location of a base-to-collector junction is defined by the trench.

4. The method of claim 1 wherein the step of forming an isolation region includes the steps of:

forming a layer of isolation material on the epitaxial layer, the layer of base material, and the layer of base protection material; and

etching a portion of the layer of isolation material to expose a portion of the layer of base protection material.

5. The method of claim 1 wherein the layer of base material includes silicon and germanium.

6. The method of claim 1 wherein the layer of base material includes silicon, germanium, and carbon.

7. The method of claim 1 and further comprising the steps of:

forming a layer of conductive material on the portion of the layer of base material and the isolation region; and

etching the layer of conductive material to form an extrinsic emitter, the extrinsic emitter contacting the portion of the layer of base material and the top surface of the isolation region.

8. The method of claim 7 and further comprising the step of planarizing the layer of conductive material prior to the step of etching the layer of conductive material.

9. The method of claim 7 wherein the step of etching the layer of conductive material is a timed etch.

10. The method of claim 7 wherein the extrinsic emitter has an end that contacts the intrinsic base region, the end having a substantially vertical end wall.

11. The method of claim 7 and further comprising the steps of:

etching the isolation region such that a side wall of the extrinsic emitter and a side wall of the isolation region are substantially aligned;

forming a first layer of insulation material on the intrinsic base region and the extrinsic emitter;

forming a second layer of insulation material on the first layer of insulation material;

etching the second layer of insulation material to form a side wall spacer that adjoins the extrinsic emitter;

etching the first layer of insulation material to remove the first layer of insulation material from the intrinsic base region;

forming an extrinsic base region in the layer of base material after the first layer of insulation material has been formed; and

forming an intrinsic emitter region in the layer of base material after the extrinsic base region has been formed.

12. The method of claim 11 wherein a width of the extrinsic emitter is less than a width of the isolation region, the width of the extrinsic emitter and the width of the isolation region being measured along a line substantially perpendicular to a plane that includes substantially all of a side wall of the extrinsic emitter.

13. The method of claim 7 wherein the layer of conductive material is polysilicon.

14. The method of claim 13 wherin the layer of conductive material is doped to have the first conductivity type.

15. The method of claim 11 wherein the step of forming an intrinsic emitter region includes the step of annealing the wafer to cause dopants to outdiffuse from the extrinsic emitter into the intrinsic base region.

16. A bipolar transistor formed on a wafer, the wafer having a buried layer and an epitaxial layer of a first conductivity type formed over the buried layer, the epitaxial layer having a top surface and a smaller dopant concentration than the buried layer, the transistor comprising:

an intrinsic base region of a second conductivity type formed on the epitaxial layer, the intrinsic base region including silicon and germanium, and having a first top surface and a vertically spaced-apart second top surface;

an isolation region formed on the first top surface of the intrinsic base region and over the second top surface of the intrinsic base region, the isolation region having a side wall;

an extrinsic emitter region formed on the isolation region and the intrinsic base region, the extrinsic emitter region having a side wall that is substantially aligned with the side wall of the isolation region; and

an intrinsic emitter region formed in the intrinsic base region, the intrinsic emitter region contacting the extrinsic emitter region.

17. The bipolar transistor of claim 16 wherein the intrinsic base region further includes carbon.

18. The bipolar transistor of claim 17 and further comprising an insulation region formed on the second top surface of the intrinsic

base region, the insulation region having a top surface substantially coplanar with the first top surface.